EPTC 2025

27th Electronics Packaging Technology Conference
2nd – 5th Dec 2025, Singapore

IEEE EPS Flagship Conference in Asia Pacific Region

Call For Papers

ABOUT EPTC

The 27th IEEE Electronics Packaging Technology Conference (EPTC2025) is an international event organized by the IEEE RS/EPS/EDS Singapore Joint Chapter and co-sponsored by the IEEE Electronics Packaging Society (EPS). Since its inauguration in 1997, EPTC has been established as a highly reputable international electronics packaging conference and is the IEEE EPS flagship conference in the Asia and Pacific Region. It aims to cover the complete spectrum of electronics packaging technology. Topics include components, materials, equipment technology, assembly, reliability, interconnect design, device and systems packaging, heterogeneous integration, wafer-level packaging, flexible electronics, LED, IoT, 5G, emerging technologies, 2.5D/3D integration technology, smart manufacturing, automation, and AI. EPTC2025 will feature keynotes, technical sessions, invited talks, panels, workshops, exhibitions, and networking activities.

The EPTC technical program committee, with more than 100 experts from diverse semiconductor packaging technology areas, is committed to creating an engaging technical program for the international packaging community. The technical program will be supplemented by an exhibition, which provides an opportunity for leading companies to exhibit their latest technologies and products. Last year there were more than 650 attendees. This year we will continue to have a 4-day (2nd ~5th Dec. 2025) program and expect more attendees.

CONFERENCE TOPICS

You are invited to submit abstract(s) on new research findings and developments in the following packaging topics:

Advanced Packaging: Flip-chip, 2.5D & 3D, embedded passives & actives on substrates, chiplets, System in Packaging, embedded chip packaging technologies, panel-level packaging, RF, microwave & millimeter-wave, Power and Rugged Electronics Packaging, advanced packaging solutions for 5G, IoT, cloud computing, autonomous vehicles, antennas, sensors, power transfer, EM shielding, RF to THz communications.

TSV/Wafer Level Packaging: Wafer-level packaging, embedded chip packaging, 2.5D/3D integration, Silicon, SiC & Glass interposer, CoWoS, FoCoS, InFo, eWLB, Embedded Multi-die Interconnect Bridge (EMIB), bumping technologies.

Interconnection Technologies: Au/Ag/Cu/Al wire-bond / wedge bond technology, Flip-Chip & Cu pillar, solder alternatives, Cu to Cu, wafer-level bonding & die attachment (Pb-free), Fan-out, panel-level, chiplets, SiP, micro-bump, high I/O thermo-compression/hybrid bonding, fine-pitch/multi-layer RDL, printable interconnects, conductive/ non-conductive adhesives, low-temperature solder, interconnects design and technology for emerging applications.

Emerging Technologies: Novel and unique packaging and material technologies for soft and intelligent packaging, flexible hybrid electronics, implantable biosensors and bioelectronics, packaging for extreme harsh environments, green/bio-resorbable packaging, packaging of MEMS &

NEMS, packaging for wide bandgap devices, quantum computing, electro-optical integration, AI, ML, packaging sensing and communication.

Materials and Processing: Photoresist, polymer dielectrics, solder, die-attach, underfill, substrates, lead-frames, materials for wafer & panel-level packaging; harsh environments, wafer bonding/debond materials; emerging electronic materials & processes novel solder metallurgies, molding compounds, thermal interface materials, advanced wire-bonding, conductive adhesives, PCB for advanced packaging, assembly processes using newer materials.

Assembly and Manufacturing Technology: Embedded/hybrid package manufacturing processes, warpage control and management in board-level assembly, thin die/package handling and assembly advance in flexible and printed electronics, large/ultra-large package (SiP, SIM, MCP) integration and processing, thermally enhanced packaging and assembly challenges.

Advanced Materials and Process Manufacturing Technology: Materials for advanced processes, characterization and handling, processing and characterizing materials, substrates in the large/ultra-large package (SiP, SIM, MCP) integration and processing, panel-level manufacturing and assembly, advances in high power, high frequency 5G/RF packaging, new materials and films in 3D stacking – chip to wafer, wafer to wafer bonding, collective die to wafer, challenges in heterogeneous integration and manufacturing, advancement in additive manufacturing for packaging substrates, equipment parts, chiplets – assembly challenges, materials and integration.

Electrical Simulation & Characterization: Power plane modelling, signal integrity analysis by simulations and characterization, 2D/2.5D/3D package level high-speed signal design, characterization, and test methodologies.

Mechanical Simulation & Characterization: Thermal-mechanical interaction study, moisture, fracture, fatigue, dynamic impact modelling and characterization, process modelling.

Thermal Characterization & Management: Thermal characterization and simulation, component, system and product level thermal management and characterization.

Quality, Reliability & Failure Analysis: Silicon, component, board and system-level reliability assessment, interfacial adhesion, accelerated testing, failure characterization, as well the testing technology, including HPC/AI chip testing/ integrated metrology, die level testing and thermal handling, silicon photonics and co-packaged devices testing, automotive, power/analog testing and next generation RF testing.

Advanced Optoelectronics and Displays: Design, simulation, interconnection, packaging, integration and materials for optoelectronics and novel displays - micro/mini/nano LED, foldable and flexible displays, Augmented Reality and Virtual Reality and wearable displays, Si and III-V photonics, optical sensors, interconnects, interposers, quantum device packaging, photonics SiP, free-space optical communications, waveguide, automotive photonics, 3D sensing, optoelectronic fiber coupling assembly, materials and reliability, fiber optic transceivers.

Smart Manufacturing and Packaging Equipment Technology: Smart Manufacturing in packaging, cycle time, data analytics, advanced metrology, Machine Learning, AI, and advanced equipment for assembly, packaging and handling.

IMPORTANT DATES

Online abstract submission start	March 31, 2025
Closing of abstract submission	**June 08, 2025**
Notification of acceptance	July 15, 2025
Full Manuscript Submission	**Sept 15, 2025**

Please check the conference website for the latest updates.

ABSTRACT AND PAPER SUBMISSION

You are invited to submit an abstract between 500–750 words long and clearly state the purpose, methodology, results (which must include data, drawings, graphs, or photographs), and conclusions of the work. Additional details on abstract submission can be found on the EPTC

website. Abstracts must be received by June 08, 2025. Your submission must have been cleared by your management and co-authors as applicable and include the authors' affiliations and email addresses. All submissions should be in English, either in pdf or MS Word. Please select the appropriate technical committee per your abstract content from the drop-down list of technical areas so that the right technical committee can evaluate your submission for acceptance. Accepted abstracts will be notified by July 15, 2025. At the technical review committee's or author's discretion, submitted abstracts may be considered for interactive poster presentation. The final manuscript for publication in the conference proceedings is due on September 15, 2025. The conference proceedings are an official IEEE publication, and the accepted papers that are registered and presented (oral and interactive) at EPTC will be uploaded to IEEE Xplore.

BEST PAPER AWARDS

The best oral papers from Academia, Industry and Students will receive cash awards and certificates. A best interactive paper award will also be presented. More details are available on the EPTC website.

CALL FOR PROFESSIONAL DEVELOPMENT COURSES

Experts in microelectronics packaging from industry and academia are invited to submit proposals for PDCs to pdcchair@eptc-ieee.net.

CALL FOR EXHIBITORS / SPONSORS

Details of the exhibition and sponsorship opportunities are available on the conference website. For enquiries, please email exhibition@eptc-ieee.net or sponsorship@eptc-ieee.net.

STUDENT TRAVEL GRANTS FOR EPTC

To encourage students in the electronics packaging field to actively participate in the flagship conferences of the society, several Student Travel Grants will be offered for EPTC annually. Also, to widen the representation of female students and students from underrepresented countries, at least two grants will be allocated to female student authors and one to a student from a country historically underrepresented at EPTC. Please find details on the EPTC website.

AFFILIATE MEMBERSHIP SUBSIDY PROGRAM

To encourage EPS membership and engagement with EPS, EPS has initiated an Affiliate Membership Subsidy Program whereby non-member conference registrations at EPTC and the other two EPS flagship conferences will be offered a complimentary EPS Affiliate Membership for the following year.
Please find details on the EPTC website.

If you have questions about abstract submission, please send your queries at techchair@eptc-ieee.net

For other queries, please email secretariat@eptc-ieee.net

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